Cactus® Technologies

SLC vs MLC NAND and The Impact of Technology Scaling

White paper CTWP010

Cactus Technologies Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong
Tel: +852-2797-2277
Email: sales@cactus-tech.com

Cactus USA
3112 Windsor Road
Suite A356
Austin, Texas 78703
Tel: +512-775-0746
Email: americas@cactus-tech.com

Cactus-Tech.com

01 Introduction

The development of NAND flash technology has, until recently, followed the path of traditional memory technologies, such as SRAM, DRAM, EEPROM, etc., in that each memory cell stores one bit of binary data. This type of NAND flash technology is now referred to as Single Level Cell or SLC.

In the push for higher densities and lower cost, new types of flash memory cell design that can store multiple bits of binary data per cell has been introduced recently. The most popular form of this type of NAND flash technology is now known as Multi Level Cell or MLC, which stores two bits per cell. Also available in the market is Tri Level Cell or TLC, which stores three bits per cell. The endurance of TLC is extremely low, on the order of 300 cycles; thus it is pretty much an accepted fact the TLC NAND is not suitable for industrial applications, even with the help of controller and firmware techniques to increase the endurance cycles.

Therefore, in this whitepaper, we will focus our attention on key differences between SLC vs MLC NAND and what the implications are for these two types of NAND as the technology node keeps shrinking.

02 Density and Cost Per Bit

MLC NAND flash device stores 2 bit per cell. This higher storage density means that for the same amount of storage, the memory array size for MLC devices is smaller than that for SLC devices. The smaller array size translates to smaller die size and, thus, lower cost per bit.

The area advantage for MLC, however, is not quite 2X that of SLC. The reason for this is because MLC needs more sophisticated program and read circuitry, thus resulting in slightly larger die area consumed by these circuits.

03 Device Performance

In order to store 2 bits per cell in an MLC NAND flash cell, the programming circuitry must be able to place 4 precise quantities of charge on the floating gate of the device, using pretty much the same voltage window as an SLC device. Fig. 1 shows the resulting Vt distribution for SLC vs. MLC.

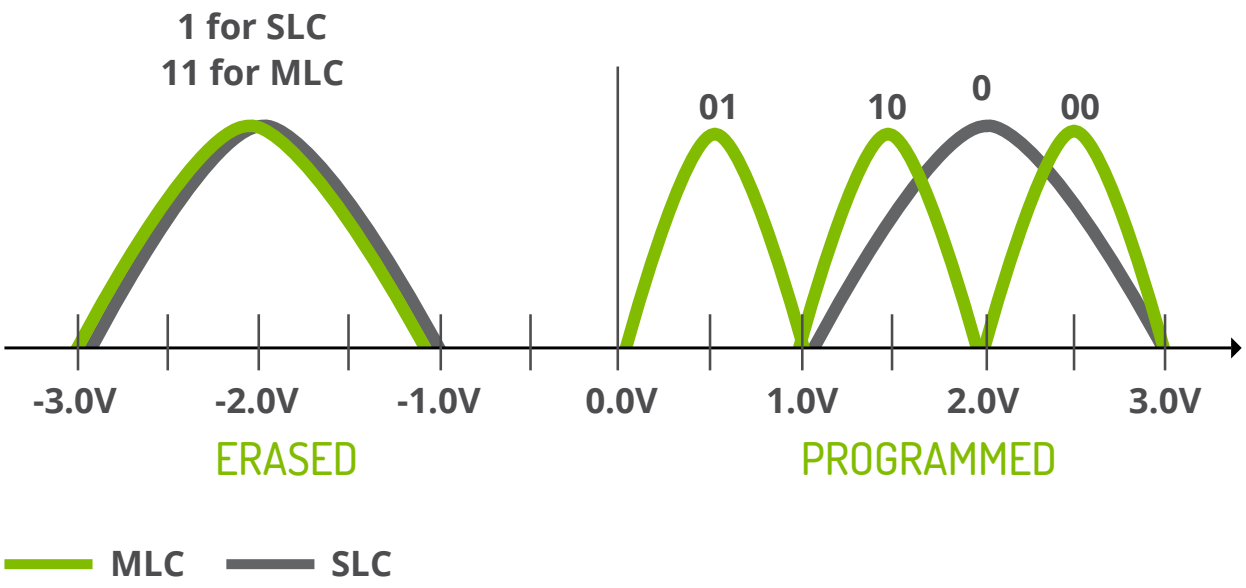


FIG. 1 SLC VS MLC Vt DISTRIBUTION

To achieve this precise distribution of charge on the floating gate of the flash device requires a more sophisticated and time consuming programming algorithm. As a result, the programming time for MLC NAND flash is up to 4X slower than that for SLC NAND flash.

A similar performance penalty exists for read operations because it takes a longer time for the read sensing circuitry to be able to distinguish between the four states accurately. Thus, the read access time for MLC NAND flash is up to 3X slower than that for SLC NAND flash.

04 System Performance

Besides the fundamental device level performance deficiencies described above, MLC NAND also suffers from lower system level performance due to lack of support for a couple of system features: copyback programming and partial programming.

Copyback programming allows the user to move a page of data from one location in the flash device to another location without having to transfer the data in and out of the memory. For a 2KByte/ page NAND flash device, this results in a time savings of over 170us per page. Copyback programming is most effective for wear leveling and read/modify/write operations.

Partial programming allows the user to program only part of a page of data in the device. For a 2KByte/page NAND flash in a typical PC application, a page of data holds 4 sectors of data. Partial programming allows the user to program one sector's worth of data at a time. This is particularly useful for read/modify/write operations or for small block transfers.

MLC NAND, due to its particular architecture and device characteristics, is more sensitive to array disturbance phenomenon. Access to part of the array can cause disturbance to other parts of the same array. Consequently, MLC NAND manufacturers have chosen not to allow partial programming or copyback programming in order to minimize the possibility of array disturbance. The lack of these two features mean that MLC NAND is slower when the user needs to move data from one location of the device to another location. It also means that MLC NAND performance in small block operations is substantially worse than SLC NAND.

05 Endurance

The process of programming a NAND flash cell results in physical damage to the thin oxide layer that separates the floating gate from the substrate. This damage accumulates over use and the net result is that, as the number of program/erase cycles increases, the voltage threshold window that separates the program state from an erase state narrows and shifts. When the erase voltage threshold shifts pass the detection threshold, it will result in read sensing error. This phenomenon is illustrated in Fig.2 for SLC NAND.

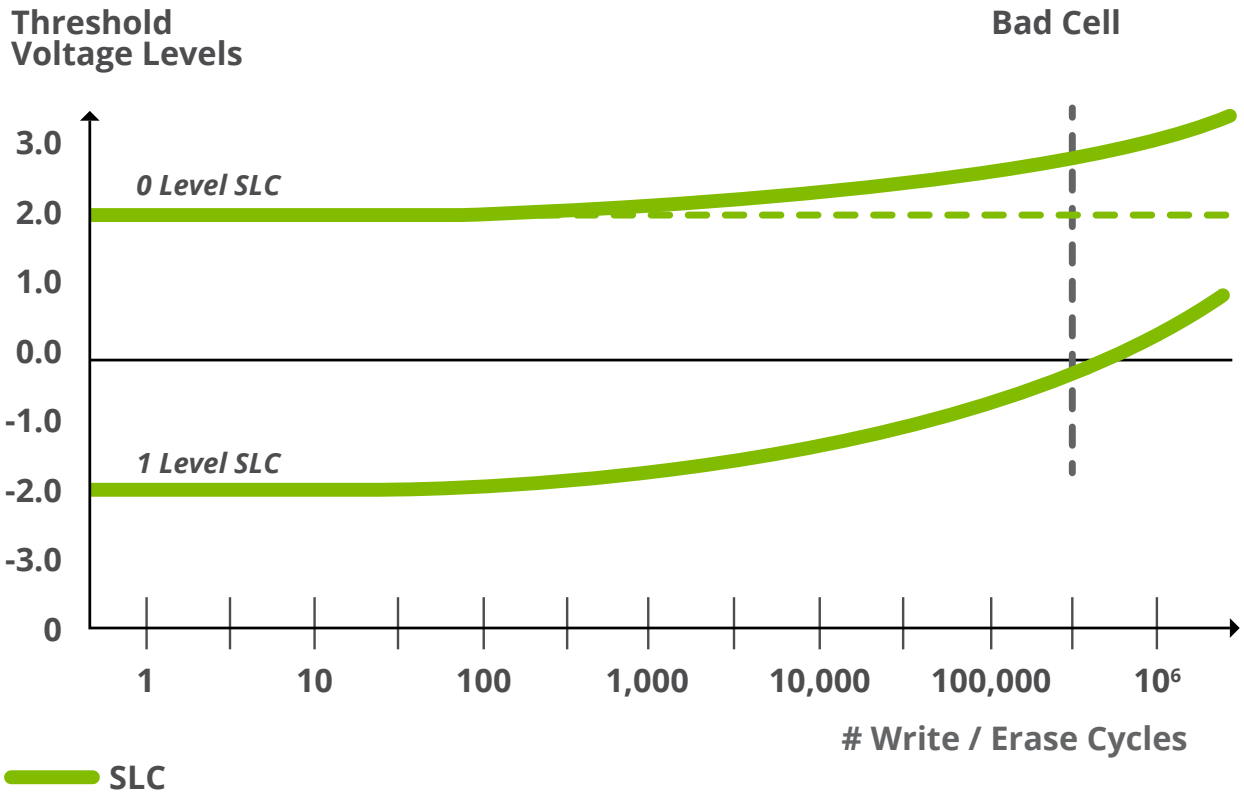


FIG. 2 SLC NAND ENDURANCE

In MLC NAND, the need to accommodate 4 distinct states within pretty much the same voltage threshold window means that for each state, the available threshold window is about 1/2 the size as compared to SLC NAND. Since the programming mechanism in MLC NAND is the same as for SLC NAND, the damage to the oxide layer during programming is the same. And since the program/erase threshold window for MLC NAND is only1/2 that of SLC NAND, this means that the effects of the program/erase window narrowing is felt much earlier for MLC NAND as compared to SLC NAND. This is illustrated in Fig.3:

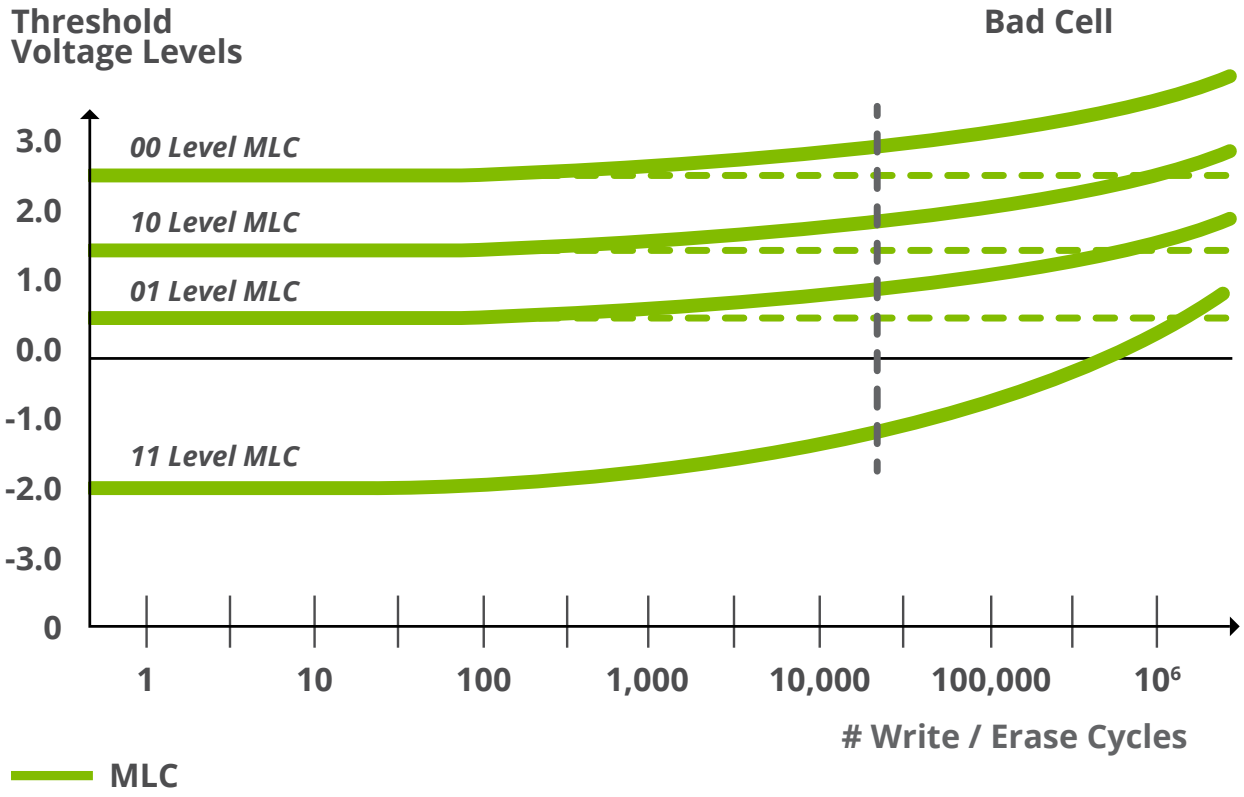


FIG. 3 MLC NAND ENDURANCE

Current SLC NAND at 4X/3Xnm technology has a minimum endurance of about 70,000 program/erase cycles per cell. In contrast, current MLC NAND at 2X/1X/1Ynm technology only has about 3,000 program/erase cycles per cell. This is more than an order of magnitude lower endurance for MLC NAND as compared to SLC NAND. This difference will only get worse as flash technology continues the march down the technology node. Fig. 4 shows the change in endurance cycles vs technology nodes:

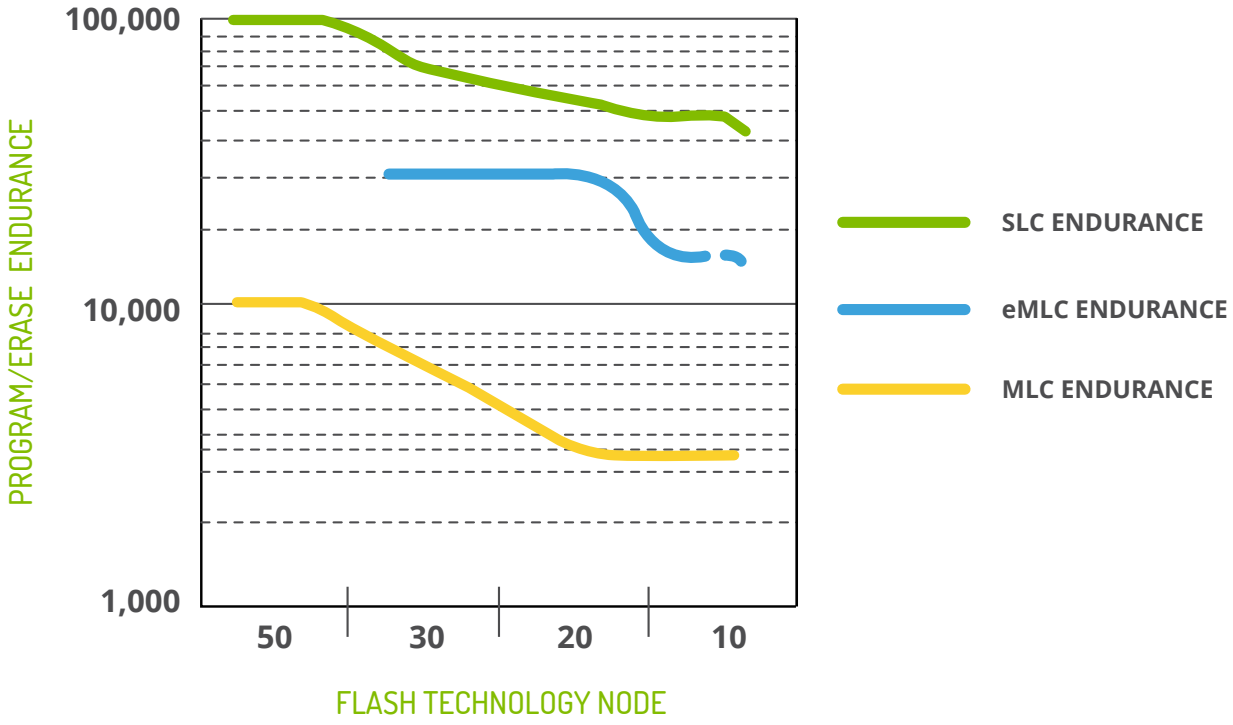


FIG. 4 NAND ENDURANCE TREND

The implication of this lower endurance limit is that MLC NAND is not suitable for applications which require frequent update of data or which require high reliability over extended operating conditions.

06 Enterprise MLC

In order to address the issue of low endurance in MLC NAND, some manufacturers offer what is known as Enterprise MLC or eMLC for short. This type of flash is manufactured identically to standard MLC flash but has a different program/erase algorithm designed to trade off performance vs endurance. eMLC offers higher endurance than standard MLC flash at the expense of lower performance. The lower performance is a result of using a more precise programming algorithm to ensure sufficient voltage margins of the programmed states.

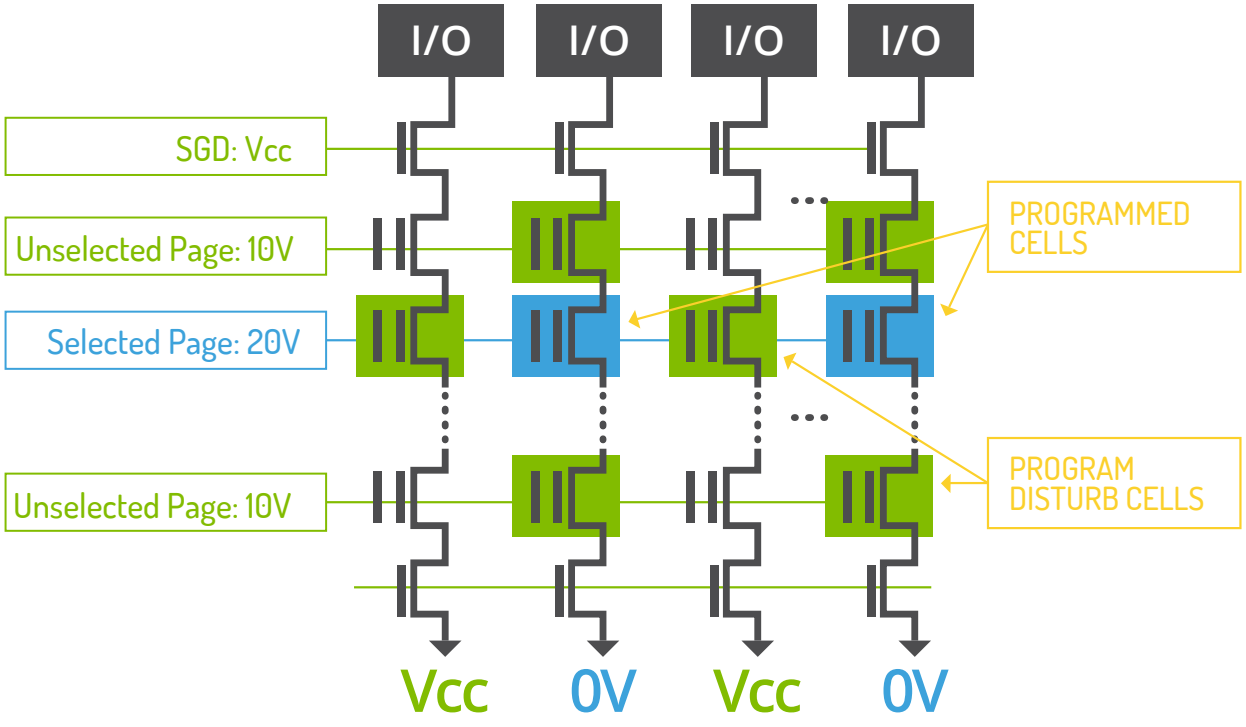
It is worth noting, however, that Fig.4 shows that the endurance of eMLC is still less than half that of SLC NAND at the same technology node. Thus, for those applications that demand long endurance and product life, SLC NAND is still the recommended choice.

07 Error Rates

As mentioned in the previous section, the voltage threshold window per state for MLC NAND is much smaller than that of SLC NAND. As a result, MLC NAND is more susceptible to read sensing errors and disturb errors. Sensing errors occur when the threshold voltage distribution shifted pass the detection threshold due to repeated program/erase cycles or due to temperature changes. Disturb errors happen due to cross coupling effects of adjacent cells in the memory array. There are two major sources of disturb errors which we will discuss below.

07.1 Program Disturb

Program disturb occurs in neighboring cells of the ones being programmed. This happens because the neighboring cells are exposed to voltage levels which are higher than normal. This setup causes these cells to appear to be weakly programmed. Fig.5 illustrations a representation of this problem:



Strings being programmed are grounded. Others are Vcc.

FIG. 5 PROGRAM DISTURB

MLC NAND is more sensitive to program disturb problems because of the smaller voltage margins per state.

07.2 Read Disturb

Read disturb happens in neighboring cells of the ones being read due to stray charge being coupled to the floating gates of the unselected cells. This problem is not as severe as write disturb but is getting worse as flash geometry shrinks. Fig. 6 illustrates this scenario:

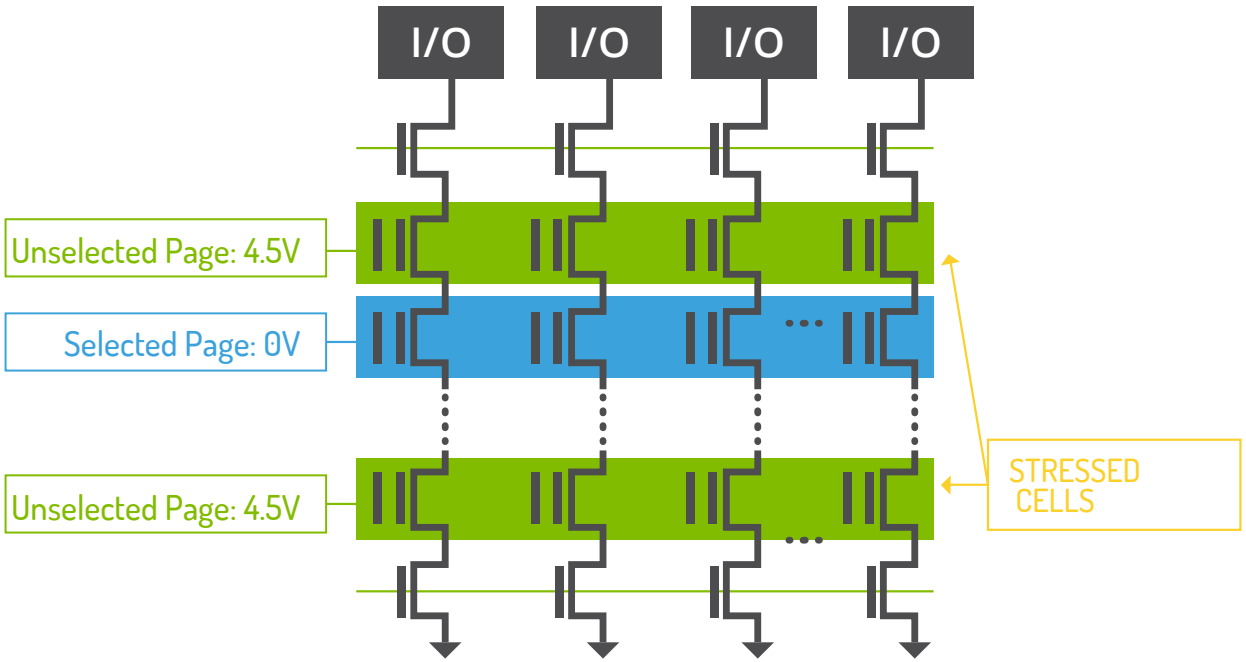


FIG. 6 READ DISTURB

07.2 Read Disturb

As is the case with endurance, both write and read disturbs get worse as the flash technology node shrinks. Fig.7 shows the relative scale of cell to cell coupling effects versus technology node:

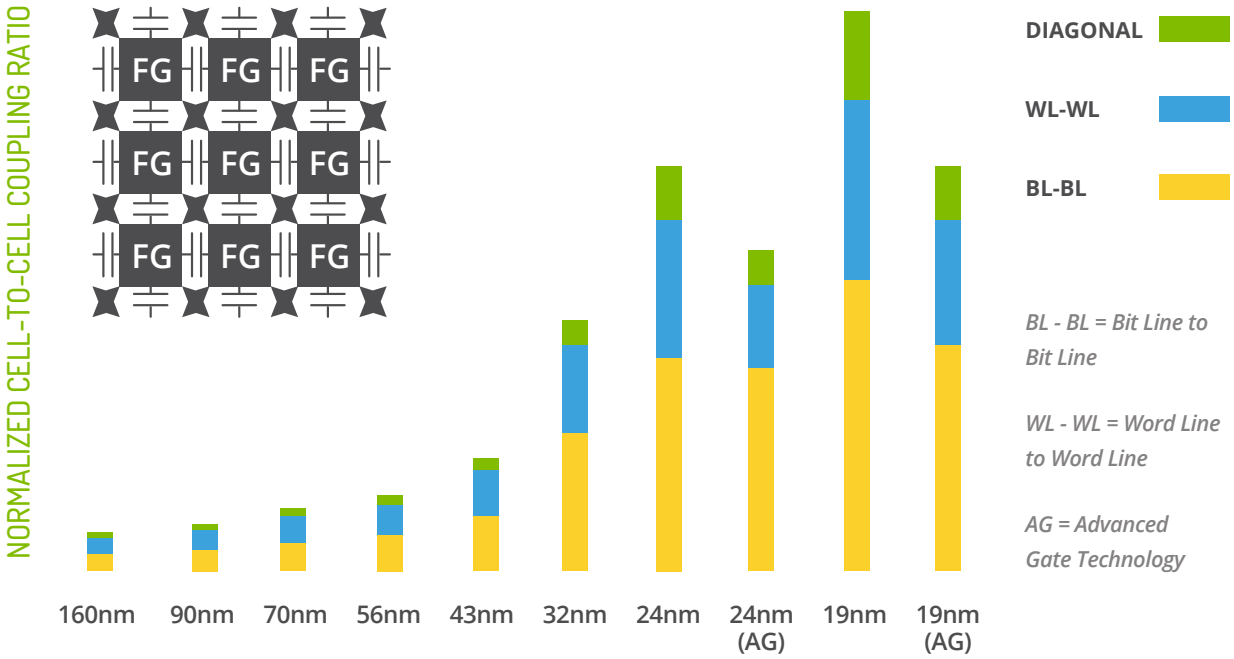


FIG. 7 CELL TO CELL COUPLING TREND

Note that currently, Cactus Technologies® uses 4X/3Xnm technology SLC NAND for our industrial grade products whereas mainstream MLC NAND is currently at 2Xnm or 1X/1Ynm. As one can see from the above graph, the cell-to-cell coupling effects of 2Xnm or 1X/1Ynm NAND is 3 to 5 times higher than for 4X/3Xnm NAND.

It is also worth noting that the effects of cell-to-cell coupling, cell leakage and voltage margin shifts are worsened for the extended voltages and temperature range environments in industrial applications.

08 Summary

In the previous sections, we have explored some of the key differences between SLC NAND and MLC NAND and how some of the key reliability parameters are affected as flash technology shrinks to smaller geometries. The important point to remember is that while MLC NAND has some advantages in terms of higher density and lower cost per bit, it suffers from low performance, low endurance and low reliability. Cactus Technologies® believes that only SLC NAND provides the superior performance, endurance and reliability required for operation in an industrial environment. Hence, Cactus Technologies® uses SLC NAND exclusively in our industrial grade flash storage products.

Controller manufacturers are aware of these shortcomings and have come up with various adaptive algorithms to compensate. With the use of these advanced algorithms, the endurance of MLC NAND can be increased up to 10X that of the raw NAND specification. This improvement may be sufficient for some applications; however, it is important to note that, from Fig. 4, even with a 10X improvement, the endurance of 1X/1Y MLC NAND is still less than half that of 4X/3X SLC NAND.

Cactus Technologies believes that only SLC NAND provides the superior performance, endurance and long term reliability required for operation in an industrial environment. Hence, Cactus Technologies uses SLC NAND exclusively in our industrial grade flash storage products.

We hope that this whitepaper has helped our customers to better understand the key differences between SLC NAND and MLC NAND. Should any of our readers have further questions on this topic, please feel free to direct your inquiries to our Sales Department.

Asia/Pac RIM info@cactus-tech.com

Americas americas@cactus-tech.com

EMEA info@cactus-tech.com